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110403

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22154 U.S. PTO  
10/701165



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Transmitted herewith for filing is the patent  
application of:

Inventors: Pierre MORIN  
Jorge Luis REGOLINI

For: SEMICONDUCTOR DEVICE WITH MOS TRANSISTORS WITH AN ETCH-STOP LAYER  
HAVING AN IMPROVED RESIDUAL STRESS LEVEL AND METHOD FOR  
FABRICATING SUCH A SEMICONDUCTOR DEVICE

Enclosed are:

Patent Application: 14 pages, 11 claims  
3 sheets of drawings  
The suggested drawing figure to be published is FIG. 3.  
Citation Under 37 CFR 1.97 and PTO-1449  
A Preliminary Amendment (with 1 replacement drawing sheets).  
Assignee info:  
Name: STMicroelectronics SA  
Address: 29, boulevard Romain Rolland, F-92120 Montrouge, France  
Country of Incorporation: France

Applicant claims priority benefit to the following foreign application(s):  
Country: France  
Application No.: 0213837  
Filing Date: November 5, 2002

The Declaration and Filing Fee are **NOT ENCLOSED**.

Name, Address and Citizenship of Inventor(s) is as follows:

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Date: November 4, 2003

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